

TSM500P02D

Taiwan Semiconductor

P-Channel Power MOSFET

-20V, -4.7A, 50mΩ

FEATURES

- Halogen-free
- Suited for 1.8V drive applications
- Low profile package

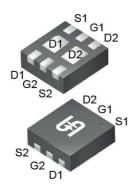
APPLICATION

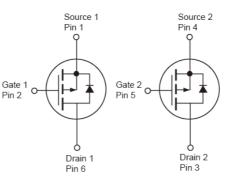
- Battery Pack
- Load Switch

KEY PERFORMANCE PARAMETERS			
PARAMETER		VALUE	UNIT
VD	S	-20	V
	V _{GS} =- 4.5V	50	
R _{DS(on)} (max)	$V_{GS} = -2.5V$	65	mΩ
	$V_{GS} = -1.8V$	85	
Q	9	9.6	nC









Notes: Moisture sensitivity level: level 3. Per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T _A = 25°C unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V _{DS}	-20	V
Gate-Source Voltage		V _{GS}	±10	V
Continuous Drain Current (Note 1)	T _C = 25°C	- I _D	-4.7	٨
	T _C = 100°C		-2.82	A
Pulsed Drain Current (Note 2)		I _{DM}	-18.8	А
Total Power Dissipation @ $T_c = 25^{\circ}C$		P _{DTOT}	0.62	W
Operating Junction and Storage Temperature Range		T _J , T _{STG}	- 55 to +150	°C

THERMAL PERFORMANCE			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction to Ambient Thermal Resistance	R _{eja}	200	°C/W

Notes: $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. $R_{\Theta JA}$ is guaranteed by design while $R_{\Theta CA}$ is determined by the user's board design. $R_{\Theta JA}$ shown below for single device operation on FR-4 PCB in still air.

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PARAMETER	CONDITIONS	SYMBOL	MIN	ТҮР	MAX	UNIT
Static (Note 3)			1			L
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_{D} = -250 \mu A$	BV _{DSS}	-20			V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	V _{GS(TH)}	-0.3	-0.6	-0.8	V
Gate Body Leakage	$V_{GS} = \pm 10V, V_{DS} = 0V$	I _{GSS}			±100	nA
Zero Gate Voltage Drain Current	$V_{DS} = -20V, V_{GS} = 0V$	I _{DSS}			-1	μA
	$V_{GS} = -4.5V, I_{D} = -3A$			42	50	mΩ
Drain-Source On-State Resistance	$V_{GS} = -2.5V, I_D = -2A$	R _{DS(ON)}		57	65	
	$V_{GS} = -1.8V, I_D = -1A$			75	85	
Forward Transconductance	$V_{DS} = -10V, I_{D} = -3A$	g _{fs}		7		S
Dynamic (Note 4)	·					
Total Gate Charge		Qg		9.6	13	nC
Gate-Source Charge	$V_{DS} = -10V, I_D = -3.0A,$	Q _{gs}		1.6	2	
Gate-Drain Charge	$V_{GS} = -4.5V$	Q _{gd}		2	4	
Input Capacitance	$V_{DS} = -10V, V_{GS} = 0V,$ - f = 1.0MHz	C _{iss}		850	1230	
Output Capacitance		C _{oss}		70	100	pF
Reverse Transfer Capacitance		C _{rss}		55	80	1
Switching (Note 5)						•
Turn-On Delay Time		t _{d(on)}		6	11	
Turn-On Rise Time	$V_{DD} = -10V,$	t _r		21.6	41	
Turn-Off Delay Time	$R_{GEN} = 25\Omega,$	t _{d(off)}		51	97	ns
Turn-Off Fall Time	$I_{\rm D} = -1$ A, $V_{\rm GS} = -4.5$ V,	t _f		13.8	26	1
Source-Drain Diode (Note 3)						
Continuous Source Current	$V_{G} = V_{D} = 0V,$	I _S			-4.7	А
Pulsed Source Current	Force Current	I _{SM}			-18.8	А
Forward On Voltage	I _S = -1.0A, V _{GS} = 0V	V _{SD}			-1.0	V

Notes:

1. Current limited by package

2. Pulse width limited by the maximum junction temperature

3. Pulse test: PW \leq 300µs, duty cycle \leq 2%

4. For DESIGN AID ONLY, not subject to production testing.

5. Switching time is essentially independent of operating temperature.



ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM500P02DCQ RFG	TDFN 2x2	3,000pcs / 7" Reel

Note:

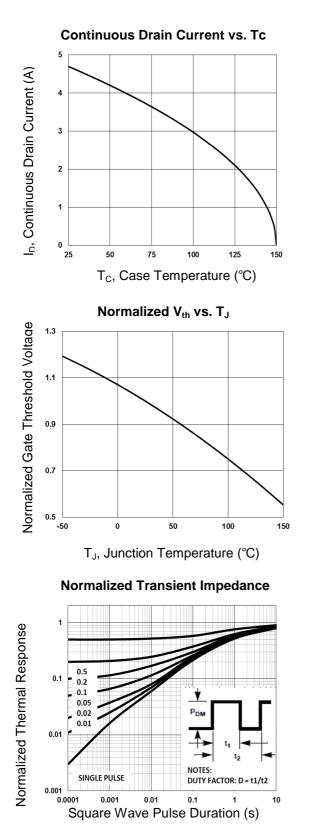
1. Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC

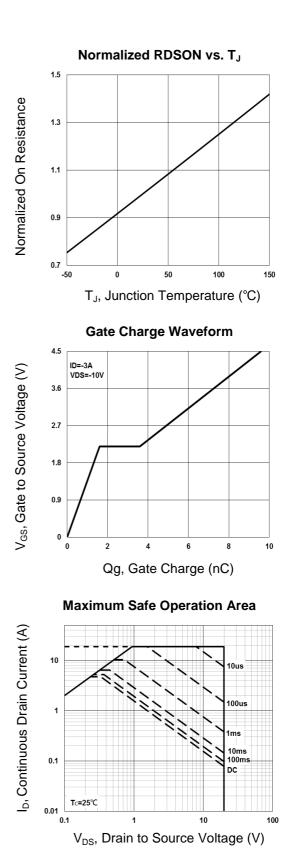
2. Halogen-free according to IEC 61249-2-21 definition



CHARACTERISTICS CURVES

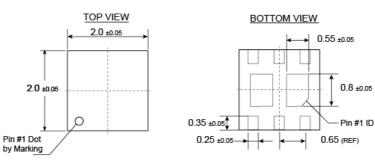
 $(T_c = 25^{\circ}C \text{ unless otherwise noted})$

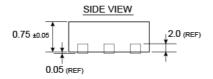




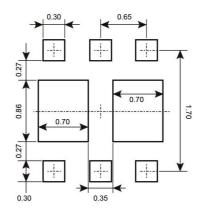








SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM

6 5 4	Y = Year Code
50P2	M = Month Code for Halogen Free Product
YML	O =Jan P =Feb Q =Mar R =Apr
	S =May T =Jun U =Jul V =Aug
I Z 3 Polarity Marking	W =Sep X =Oct Y =Nov Z =Dec
	L = Lot Code (1~9, A~Z)

TDFN2x2



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